# Name: Section:

# Homework Assignment: submit via gradescope

1. [1.2] Volume of sale (i.e., the number of parts sold) is a factor when determining which device technology is to be used. Assume that a system can be implemented by FPGA, gate array or standard-cell technology. The per-part cost is $15, $3, and $1 for FPGA, gate array, and standard cell respectively. Gate-array and standard-cell technologies also involve a one-time mask generation cost of $20,000 and $100,000 respectively.
	1. Assume the number of parts sold is *N*. Derive the equation of per-unit cost for the three technologies.
	2. Plot the equations with *N* as the x-axis. [I recommend using a program like excel]
	3. Determine the rage of *N* for which FPGA technology has the minimal per-unit cost.
	4. Determine the rage of *N* for which gate-array technology has the minimal per-unit cost.
	5. Determine the rage of *N* for which standard-cell technology has the minimal per-unit cost.
2. [1.3] What is the view (behavioral, structural, or physical) of the following illustration?



1. [1.4] What is abstraction? Why is it important for digital system design?
2. [1.5] What is the difference between testing and verification?
3. Install and test Xilinx Vivado: [Vivado Installation Instructions](https://georgeyork.github.io/ECE383_web/hand/Vivado%20Installation%20Instructions.docx)
4. Design a digital system with four bits of inputs I3 I2 I1 I0 and two bits of outputs O1 O0. At least one of the inputs is always equal to 1. The output encodes the index of the most significant 1 in the input. For example, if I3 I2 I1 I0 = 0101, then the index of the most significant 1 is 2, hence O1 O0 = 10. Hint, you will need a **don't care** somewhere. Turn in....
	1. Complete truth table.

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| --- | --- | --- |
| **Hexadecimal Digit** | **Inputs** | **Outputs** |
| **I3** | **I2** | **I1** | **I0** | **O1** | **O0** |
| **0** | 0 | 0 | 0 | 0 |  |  |
| **1** | 0 | 0 | 0 | 1 |  |  |
| **2** | 0 | 0 | 1 | 0 |  |  |
| **3** | 0 | 0 | 1 | 1 |  |  |
| **4** | 0 | 1 | 0 | 0 |  |  |
| **5** | 0 | 1 | 0 | 1 |  |  |
| **6** | 0 | 1 | 1 | 0 |  |  |
| **7** | 0 | 1 | 1 | 1 |  |  |
| **8** | 1 | 0 | 0 | 0 |  |  |
| **9** | 1 | 0 | 0 | 1 |  |  |
| **A** | 1 | 0 | 1 | 0 |  |  |
| **B** | 1 | 0 | 1 | 1 |  |  |
| **C** | 1 | 1 | 0 | 0 |  |  |
| **D** | 1 | 1 | 0 | 1 |  |  |
| **E** | 1 | 1 | 1 | 0 |  |  |
| **F** | 1 | 1 | 1 | 1 |  |  |

* 1. Two 4-variable kmaps.

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* 1. Minimal SOP expressions for O1 and O0
	2. VHDL code for the circuit (pushed to Bitbucket). Make sure that you have a proper file header. See bottom of <https://georgeyork.github.io/ECE383_web/lab/labnotebook.html>