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ECE 383 - Embedded Computer Systems II
Lecture 4 - Sequential Element

versus Combinational?

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Using Unsigned and Decimal Numbers

- **Convert Decimal number to Unsigned Vector (7 downto 0)**
  - to_unsigned(17, 8)
    - First argument is the decimal number
    - Second argument is the number of bits

17

8

answer

- **Conditional with unsigned number**

```
LED_Trigger <= '1' when (Binary_Input = to_unsigned(17, 8) ) else
        '0';
```

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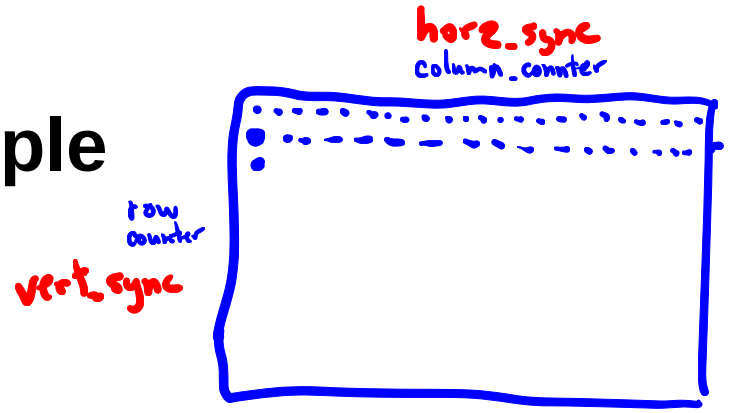
Lesson Outline

1. Sequential Elements
2. Mod 10 Counter Example
   - Truth Table
   - Timing Diagram
   - Circuit Diagram
   - VHDL
3. General VHDL Rules
4. Adding Signals to Vivado

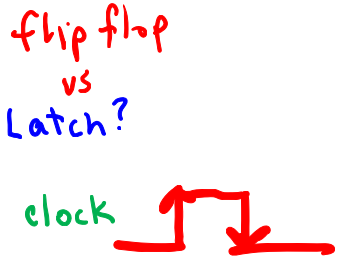
Homework #4

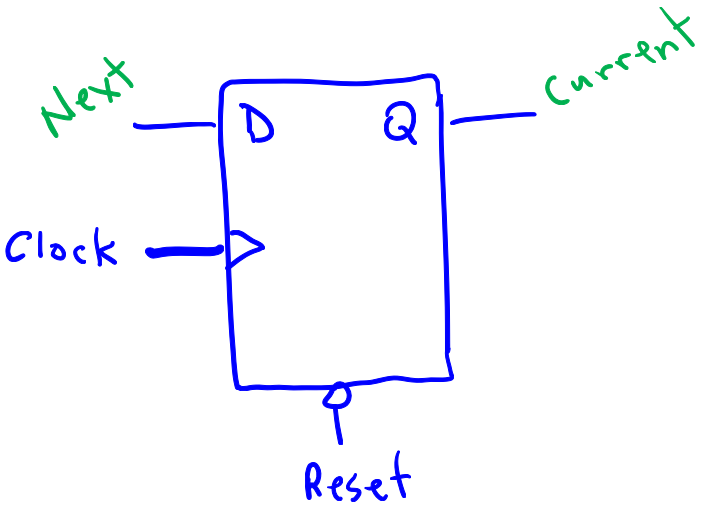


Sequential Elements

Sequential Elements

- Goals:
  - basic sequential process and sensitivity list
  - register, counter in VHDL
  - Combination of sequential and combinational logic (counters)
  - Translate between schematic, truth table, and VHDL code





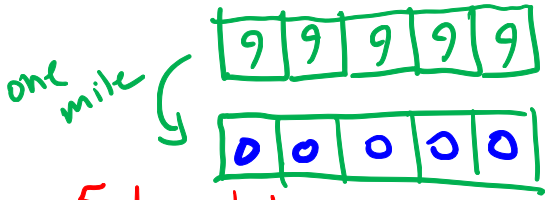
x++;
y = x mod 10;

y is between __ and __

8	10	1000
9	11	1001
A	12	1010
B	13	1011
C	14	1100
D	15	1101

Odometer

ripple?



5 decimal digits are modulo ____

y = x mod ____

4-bit counter:

2^4 =

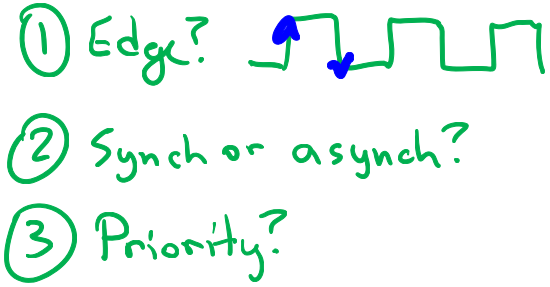
0 - F

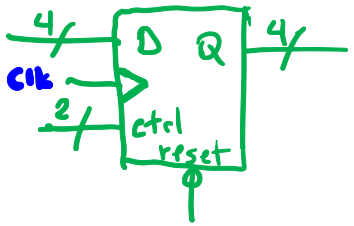
0 - 9, A - F

Mod 10 Counter Example

- Decade counter
- Base 10 counter

Mod 10 Counter Example





- **Truth Table**

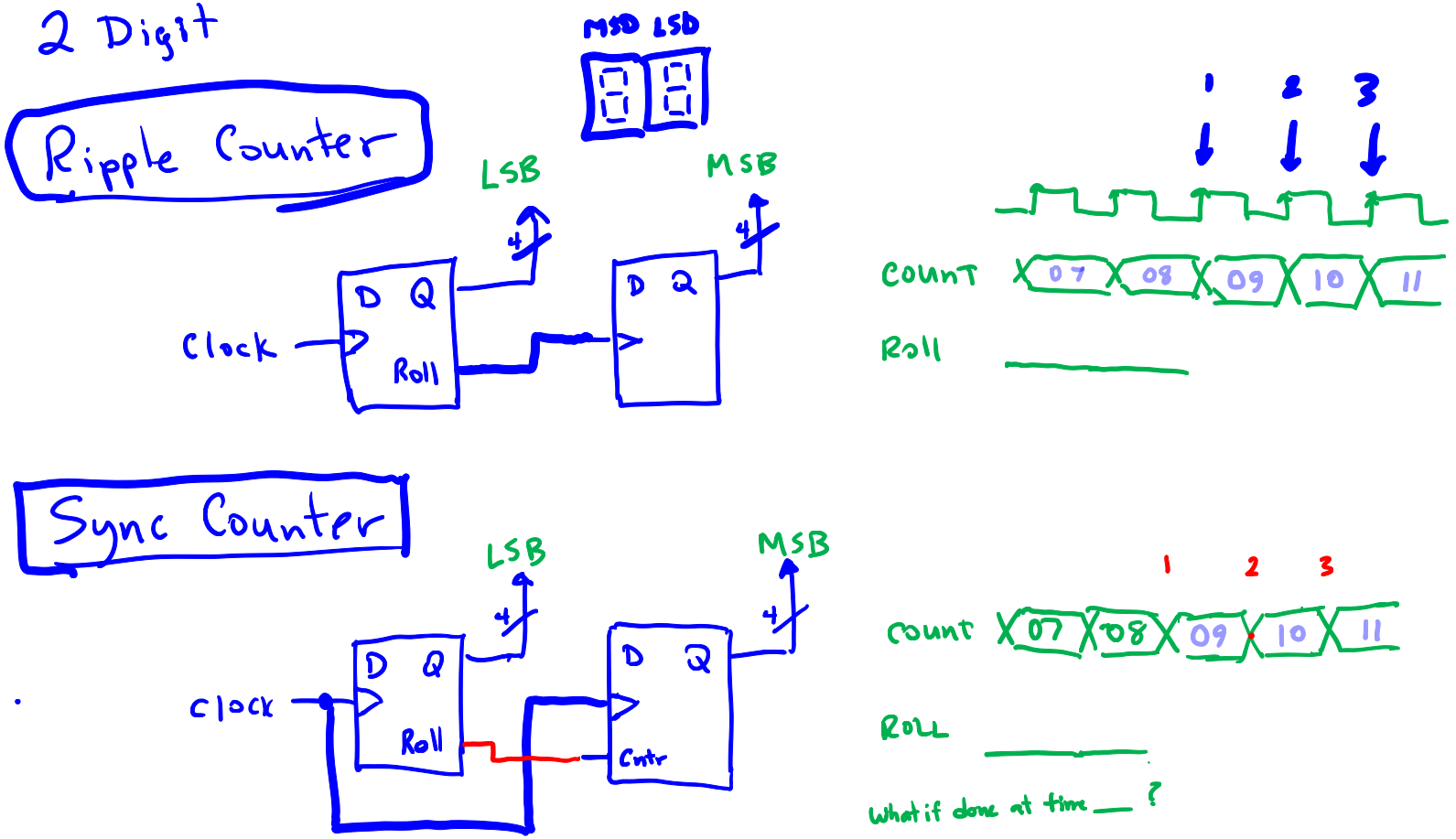
IN OUT Mode

clk	reset	ctrl	D	Q
0,1,falling	x	xx	x	Q
rising	0	xx	x	0
rising	1	00	x	Q
rising	1	01	x	(Q+1) mod 10
rising	1	10	D	D
rising	1	11	x	0

4 Why 2 resets?

Missing? — — —

Cascade Mod-10 counters?



Handout:

Complete the Q trace in the following timing diagram based on the state table for the mod-10 counter.

↳ Do Handout

Timing Diagram

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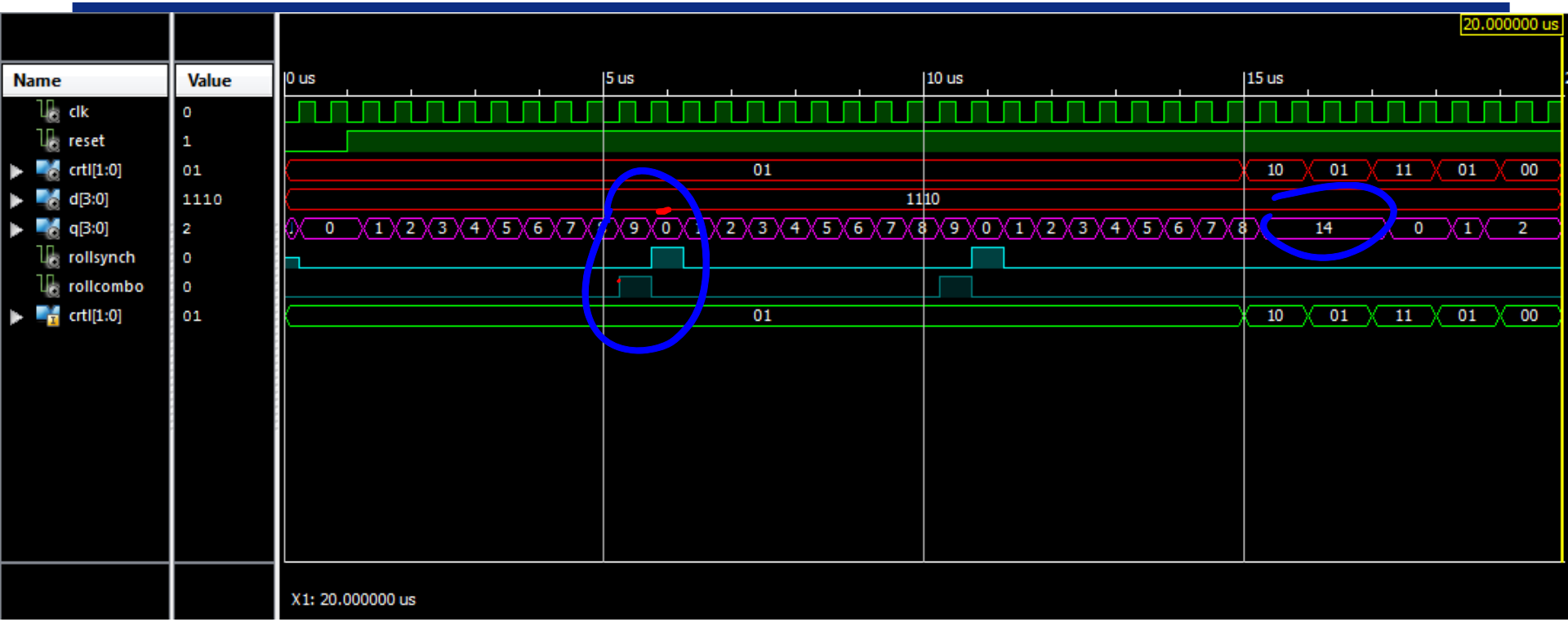
Mod 10 Counter - Timing Diagram



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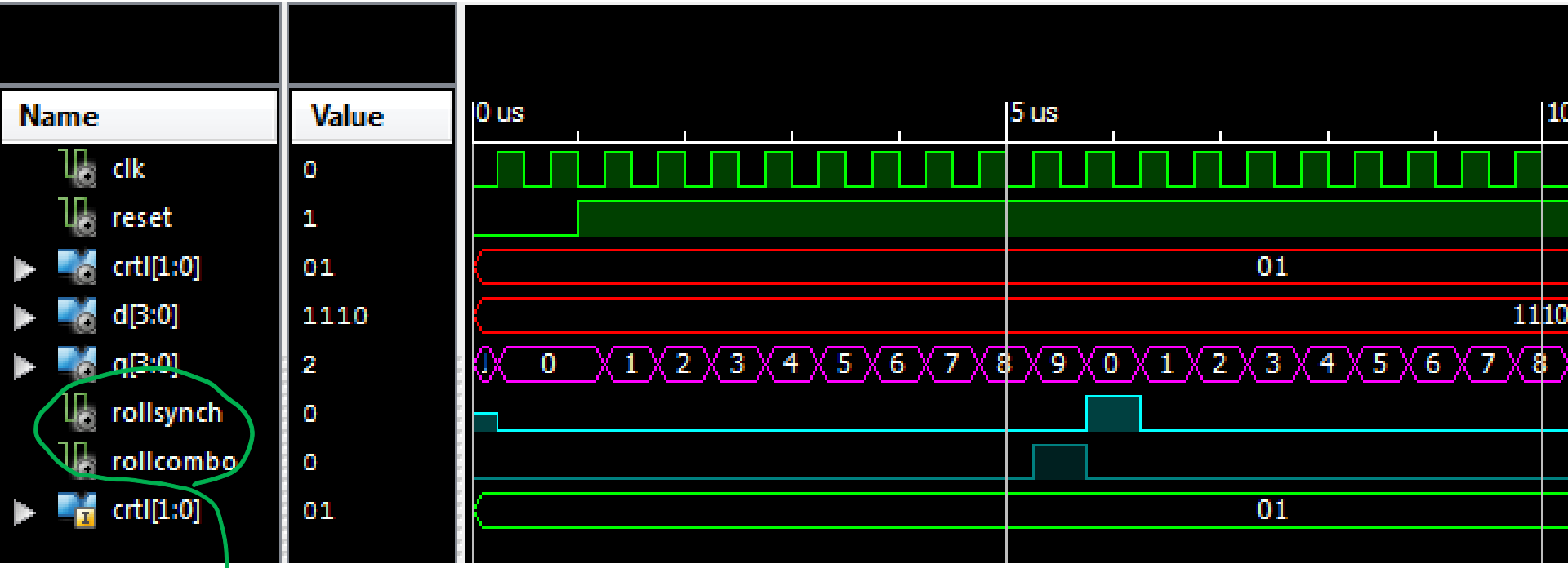
Mod 10 Counter - Timing Diagram



which is best for Ripple counter? Roll _____

for Sync counter? Roll _____

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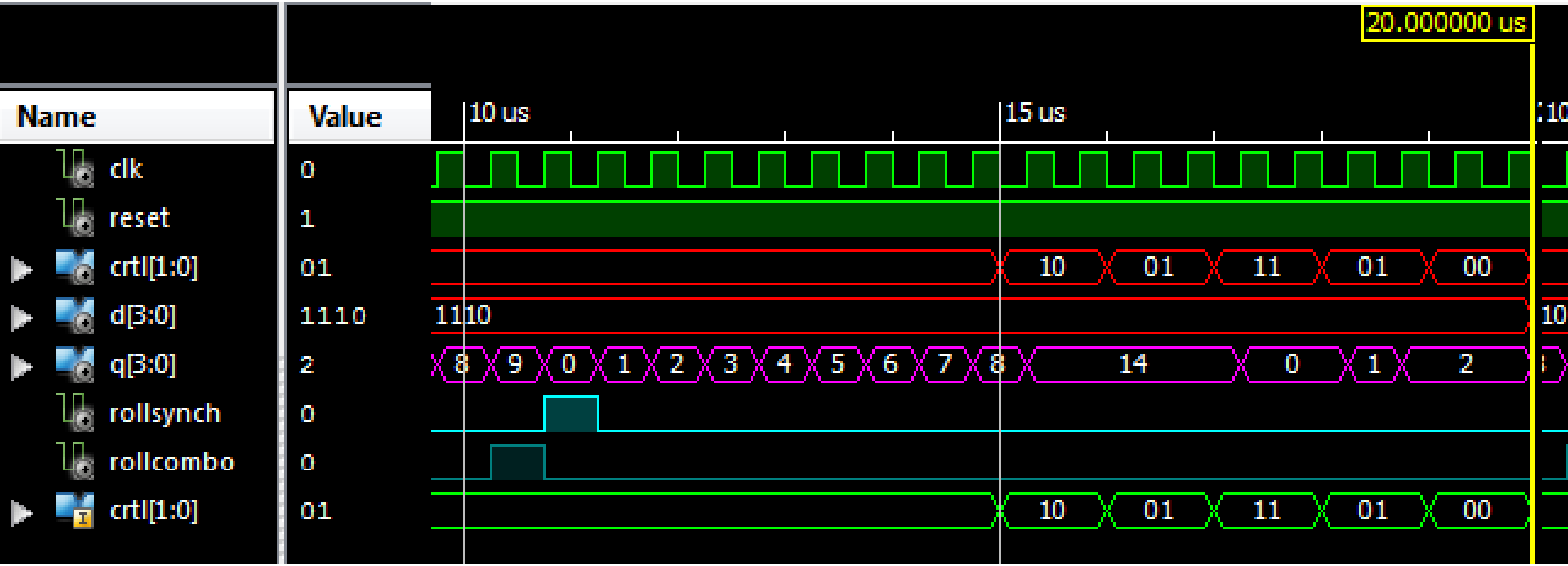
Mod 10 Counter - Timing Diagram



Circuit Diagram

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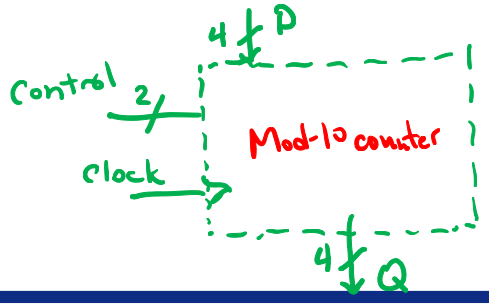
Circuit Diagram

- After completing the timing diagram, see if you can figure out how to construct the counter using the arrangement of devices show in the picture below.
  - You may assume that all these inputs are able to handle 4-bit values - to indicate this, draw a hash through the signal lines with a "4" next to it.
  - ~~You should not draw additional lines in this picture. Instead, label the wires with names and use these names to create logical connections between signals with the same name.~~
  - Draw a border around your circuit. The only signals that should cross the boundary are those which are part of the entity description.



Circuit Diagram

- **Build the Architecture for the Mod 10 Counter**

If Dr York says use
a mod-10 counter BBB to make a circuit
on a GR...

VHDL

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Mod 10 Counter – VHDL Code Entity

```
entity lec4 is
    Port(     clk: in  STD_LOGIC;
              reset : in  STD_LOGIC;
              ctrl: in std_logic_vector(1 downto 0);
              D: in unsigned (3 downto 0);
              Q: out unsigned (3 downto 0));
end lec4;
1.  architecture behavior of lec4 is

2.      signal rollSynch, rollCombo: STD_LOGIC;
3.      signal processQ: unsigned (3 downto 0);

4.  begin
```

Mod 10 Counter – VHDL Code Architecture

```
5.  process(clk)
6.    begin
7.        if (rising_edge(clk)) then
8.            if (reset = '0') then
9.                processQ <= (others => '0');
10.               rollSynch <= '0';
11.           elsif ((processQ < 9) and (ctrl = "01")) then
12.               processQ <= processQ + 1;
13.               rollSynch <= '0';
14.           elsif ((processQ = 9) and (ctrl = "01")) then
15.               processQ <= (others => '0');
16.               rollSynch <= '1';
17.           elsif (ctrl = "10") then
18.               processQ <= D;
19.           elsif (ctrl = "11") then
20.               processQ <= (others => '0');
21.           end if;
22.       end if;
23.   end process;
24.   rollCombo  <= '1' when (processQ = 9) else '0';
25.   Q <= processQ;
26. end behavior;
```

Roll Issue (Bug) with RollCombo

"01" count up
"00" hold

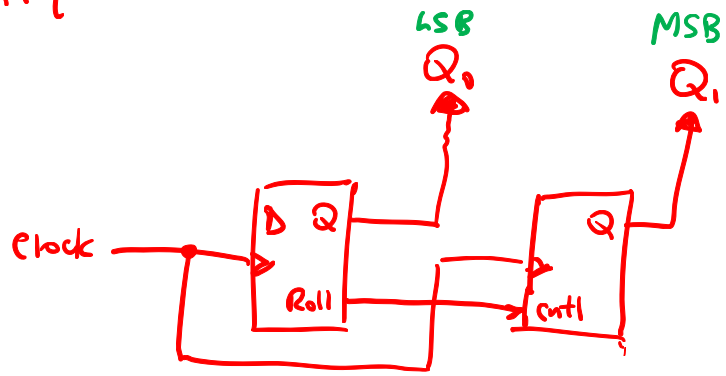
Q	7	8	9	9	0	1	2
Crtl	01	01	00	01	01	01	

Roll combo

fixed Roll Combo

If 2 Cascaded Synch Counters

			Hold	count		
Ideal Q_1Q_0	07	08 09	09	10	11	12
Actual Q_1Q_0	07	08 09	—	—	—	—



General VHDL Rules

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General VHDL Rules

- Introduce the following rules for designing in VHDL in order to write code that can be **synthesized**.
  - Never use processes for combinational logic.
  - Only the clk should appear in the sensitivity list
  - The outermost structure should be "if (rising_edge(clk)) then"
  - Inside this structure should be "if (reset = '0') then" to reinitialize the state element used by the process
  - The else clause of the reset element (the body) should consist of a set of **exclusive** signal conditions in an if/then case structure.
  - Any signal on the **left-hand** side of an assignment statement (in the body) may not be put on the **left-hand** side of any assignment statement outside the process.

Adding Signals in Vivado

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Adding Signals in Vivado

- Sometimes it is necessary to examine signals not directly visible in a design. In the Instances and Process subwindow, reveal the instances inside the lec4_tb by clicking on the arrow to the left lec4_tb.
  1. Reveal the signals inside the lec4 instance (called uut) by clicking on the label "uut".
  2. In the Objects subwindow select the signal that you want to observe on the timing diagram. In our case the ctrl signal.
  3. Drag and drop the signal into the timing diagram.
  4. In most cases you will have to restart the simulation to get a complete trace of the newly added signal.
  5. And the rerun it for the needed amount of time.

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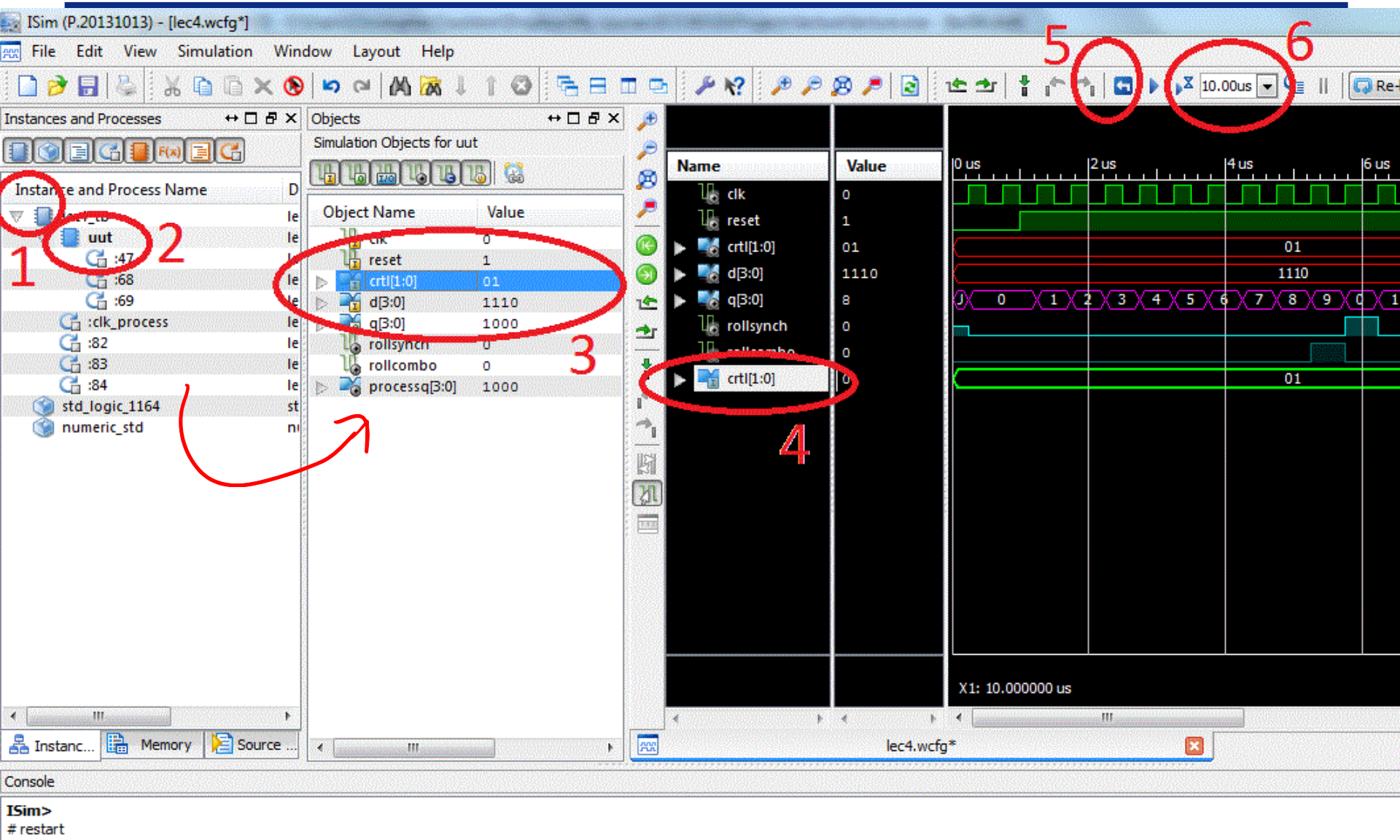
Adding Signals in Vivado Simulator



HW#4

go to Hw4.pdf

- power switch
- USB cable
- Driver not installed